Please amend the abstract as follows:

There is provided the reproduction signal processor in which the power consumption in the equalization is reduced without lowering the equalization performance, and which corresponds also to the high-speed ~~reproduction.~~

~~The reproduction signal processor comprises the straight-line interpolation unit (6), in order to~~ reproduction. The reproduction signal processor comprises the straight line interpolation unit (6), in order to perform equalization by using the frequency-divided clock as the operation clock as well as compensate information which is omitted due to the use of the frequency-divided clock.